REMARKS/ARGUMENTS

This paper is being provided in response to the June 17, 2004 Final Office Action for the above-referenced application. In this response, Applicant has cancelled Claims 4, 20, and 34, and amended Claims 1, 5, 8, 12, 14, 16, 18, 19, 21, 22, 25, 26, 31, 32, 33, 35 in order to clarify that which Applicant deems to be the claimed invention. Applicant respectfully submits that the amendments to the claims are all supported by the originally filed application.

Applicant thanks the Examiner for the indication of the allowability of Claims 8-11 if rewritten in independent form including all the limitations of the base claim and any intervening claims. Accordingly, Applicant has rewritten Claims 8-11 in accordance with the foregoing remarks set forth in the Office Action and requests that the objection be reconsidered and withdrawn. Applicant respectfully submits that Claims 8-11, as amended herein, are now in condition for allowance.

In response to the objection to the Abstract, Applicant has amended the Abstract in accordance with remarks set forth in the Office Action. Accordingly, Applicant respectfully submits that the objection be reconsidered and withdrawn.

In response to the objection to Applicant's previously submitted replacement drawings, Applicant submits herewith new replacement Figures 1-14 incorporating those corrections previously presented to, and approved by, the Examiner. Applicant respectfully submits that the new drawings do not add any new matter. Accordingly, Applicant respectfully requests that this objection be reconsidered and withdrawn.

In response to the objection to the drawings under 37 1.83(a), Applicant has amended Claims 25 and 26 herein in accordance with remarks set forth in the Office Action. Specifically, Applicant has amended Claims 25 and 26 to recite that the specialized hardware, as claimed, performs functions of the previously recited first hardware, second hardware, third hardware and fourth hardware. Accordingly, Applicant respectfully requests that the rejection be reconsidered and withdrawn.

In response to the objections to the specification, Applicant has amended the specification in accordance with remarks set forth in the Office Action. Further, in connection with the amendment to the paragraph located on page 21, beginning at line 19, at line 6 of that paragraph, Applicant has amended this portion of the paragraph to read "the buses 26, 28, or through some means (not ~~shown~~ illustrated in Fig. 14)". Applicant respectfully submits that one of ordinary skill in the art will appreciate that the hardware 152 may receive access requests using other elements besides the particular buses 26 and 28 illustrated.

The Office Action also states, in connection with the paragraph beginning at page 9, line 10, at line 11 of the paragraph, that "is" appears to read more clearly here as –must be- . Applicant submits that the suggested change is not necessary and the paragraph is clear without making the forgoing amendment.

In response to the objection to the specification as failing to provide proper antecedent basis for the claimed subject matter, Applicant has amended the specification and respectfully requests that the objection be reconsidered and withdrawn.

In particular, the Office Action states that the specification does not provide an adequate written description of a computer program product which is stored on a "computer readable medium" and does not appear to provide any antecedent basis for "machine executable code." In this response, Applicant has amended the specification to provide an antecedent basis for "machine executable code", as recited in Applicant's claims, by including in the Description a paragraph similar to that which is included in the Summary of the Invention. Applicant respectfully submits that no new matter has been entered since the paragraph was included in Applicant's originally filed specification in the Summary of the Invention section.

The disclosure of "machine executable code" indicates that the code is executed on a processor. For code, "machine executable" can only mean executable on a processor. Applicant notes that for code to be ***machine executable***, the code must be at some point stored in a computer readable medium. Although code may arguably also be located in a place other than on a computer readable medium, for code to be ***machine executable***, it is stored on a computer readable medium. Thus, Applicant respectfully submits that machine executable code provides that the code is executed by a computer and embodied on a computer readable medium.

Furthermore, Applicants respectfully submit that M.P.E.P. §2106 IIC provides, in part, that:

> Claims and disclosures are not to be evaluated in a vacuum. If elements of an invention are well known in the art, the applicant does not have to provide a disclosure that describes those elements. In such a case, the elements will be construed as encompassing any and every art recognized hardware or combination of hardware and software techniques for implementing the defined requisite functionalities.

Applicant respectfully submits that the term "machine executable code" should not be evaluated in a vacuum and that, the term "machine executable code", as recited in Applicant's claims, and included in the Summary of the Invention and the Description, is understood to include the well-known features of a computer readable medium to store the executable code as well as a computer to execute the "machine executable code". Without both the well known computer readable medium and computer, "machine executable code" would not be executable.

In view of the foregoing, Applicant respectfully requests that this objection be reconsidered and withdrawn.

In response to the objections to the Claims, Applicant has amended the Claims in accordance with remarks set forth in the Office Action. Accordingly, Applicant respectfully requests that the rejection be reconsidered and withdrawn.

In response to the rejection of Claims 19-28, Applicant has amended the claims herein. In particular, Applicant has amended Claim 19 to clarify "the requested data" and to clarify use of the second access balancing technique.

The Office Action states that it is not clear how Claim 22 limits Claim 20 since it appears to be encompassed within the language of Claims 18 and 19. Applicant respectfully submits that Claim 22 recites additional features regarding the implementation of the first and second balancing techniques. Claim 18 does not recite this feature regarding the implementation of first and second balancing techniques. Claim 18, at lines 6-9, recites that the system includes cache selection hardware for selecting a cache memory for use in accordance with an access balancing

technique, but Claim 18 does not recite additional features of Claim 22 regarding how the access balancing technique is implemented.

In connection with the rejection of Claims 25 and 26 under 112, second paragraph, Applicant has amended the claims to remove recitation of first hardware, second hardware, third hardware, and fourth hardware which appears to serve as the basis for this rejection.

In view of the foregoing, Applicant respectfully requests that the rejection be reconsidered and withdrawn.

The rejection of Claims 31-41 under 35 U.S.C. § 112, ¶1 is hereby traversed and reconsideration there of is respectfully requested.

The Office Action states that the specification does not provide an adequate written description of a computer program product which is "stored on a computer readable medium". For reasons set forth above in connection with the response to the objection of the specification regarding "machine executable code" and "computer readable medium", Applicant respectfully submits that the specification provides an adequate written description of a computer program product "stored on a computer readable medium" as set forth in Claims 31-41.

Accordingly, Applicant respectfully requests that this rejection be reconsidered and withdrawn.

The rejection of Claims 1-2, 4-7, 12-32 and 34-37 under 35 U.S.C. § 103(a) as being unpatentable over Dewey et al. (U.S. Patent No. 5,724,501, hereinafter referred to as "Dewey") in view of Kurokawa et al. (U.S. Patent No. 6,571,350, hereinafter referred to as "Kurokawa") is hereby traversed and reconsideration thereof is respectfully requested. Applicant respectfully submits that Claims 1-2, 4-7, 12-32 and 34-37, as amended herein, are patentable over the cited references.

Applicant's Claim 1, as amended herein, recites a method of managing data in a cache, comprising: providing a first cache memory containing data; providing a second cache memory containing data, wherein at least some of the data contained in the first cache memory is the same as at least some of the data contained in the second cache memory, wherein data contained in said first and said second cache memories includes control data and corresponding disk data, said control data being replicated in said first and said second cache memories independent of whether said corresponding disk data is included in both said first and said second cache memories; and in response to a request for data that is stored in both the first cache memory and the second cache memory, selecting which one of the first and second cache memories to use to obtain the requested data in accordance with an access balancing technique.

Claims 2, 4-7, and 12-17 depend from Claim 1.

Applicant's Claim 18, as amended herein, recites a system for managing data in a cache comprising: a first cache memory containing data; a second cache memory containing data wherein at least some of the data contained in the first cache memory is the same as at least some of the data contained in the second cache memory, wherein data contained in said first and said

second cache memories includes control data and corresponding disk data, said control data being replicated in said first and said second cache memories independent of whether said corresponding disk data is included in both said first and said second cache memories; and cache selection hardware for selecting, in response to a request for requested data that is stored in both the first cache memory and the second cache memory, which one of the first and second cache memories to use to obtain the requested data in accordance with an access balancing technique. Claims 19-30 depend from Claim 18.

Applicant's Claim 31, as amended herein, recites a computer program product stored on a computer readable medium for managing data in a cache, comprising: machine executable code for providing a first cache memory containing data; machine executable code for providing a second cache memory containing data, wherein at least some of the data contained in the first cache memory is the same as at least some of the data contained in the second cache memory, wherein data contained in said first and said second cache memories includes control data and corresponding disk data, said control data being replicated in said first and said second cache memories independent of whether said corresponding disk data is included in both said first and said second cache memories; and machine executable code for, in response to a request for data that is stored in both the first cache memory and the second cache memory, selecting which one of the first and second cache memories to use to obtain the requested data in accordance with an access balancing technique. Claims 32, and 34-37 depend from Claim 31.

Dewey relates to improvements in fault tolerant data processing systems and methods. (Col. 1, Lines 6-7). To facilitate quick recovery of data lost as a result of a controller of cache

failure, the memory module associated with a failed controller is placed in a failover mode in which data is recovered in two stages using a battery backup. (Col. 4, Lines 15-21). Upon a controller failure, the metadata is first copied to a backup controller over a serial link. During a secondary recovery stage, the backup controller processes new host commands in the foreground and fetches mirrored data from the failed cache in the background. (Col. 4, Lines 29-37).

Kurokawa discloses a data handling system having a redundant storage configuration. (Col. 1, Lines 8-9). Kurokawa's Figure 1 includes duplicate data storage in separate storage units SU(0) 16 and SU(1) 26. One of the storage units SU(0) and SU(1) performs as a master and the other as a sub storage in accordance with each address. (Col. 4, Lines 57-63; Figure 1). The master storage regions and sub storage regions are interleaved. (Col. 5, Line 65-Col. 6, Line 5; Figure 2). Kurokawa's Figure 8 includes a work storage WS unit in each of SU(0) and SU(1). Each WS is a cache memory smaller than the main storage which retains copies of a part of data in the main storages. Given a store or fetch request, the storage unit SU(0) or SU(1) stores or fetches data directly to or from the WS(0) or WS(1) when the WS(0) or WS(1) contains the desired data to be referenced. When the desired data is not found in WS(0) or WS(1), the storage SU(0) or SU(1) fetches a block of data including the desired data from the MS(0) or MS(1) and transfers the block in the WS. The storage unit SU(0) or SU(1) again accesses the WS(0) or WS(1) for a fetch or a store operation. (Col. 9, Line 60-Col. 10, Line 27; Figure 8).

Applicant's Claim 1, as amended herein, is neither disclosed nor suggested by the references in that the references, taken separately or in combination, neither disclose nor suggest ***a method of managing data in a cache, comprising: providing a first cache memory containing data; providing a second cache memory containing data, wherein at least some of***

the data contained in the first cache memory is the same as at least some of the data contained in the second cache memory, wherein data contained in said first and said second cache memories includes control data and corresponding disk data, said control data being replicated in said first and said second cache memories independent of whether said corresponding disk data is included in both said first and said second cache memories; and in response to a request for data that is stored in both the first cache memory and the second cache memory, selecting which one of the first and second cache memories to use to obtain the requested data in accordance with an access balancing technique, as set forth in Claim 1. Dewey discloses handling write data in a mirrored fashion writing the write data to two memories, and using a non-mirrored-caching technique for data written to cache in response to a host read request. Thus, Dewey appears silent regarding any disclosure or suggestion of replicating control data in two cache memories independent of whether corresponding disk data is stored in both cache memories. Kurokawa also appears silent with regard to any disclosure or suggestion of replicating control data in two cache memories independent of whether corresponding disk data is stored in both cache memories. Accordingly, the references neither teach, disclose nor suggest at least the feature of ***wherein data contained in said first and said second cache memories includes control data and corresponding disk data, said control data being replicated in said first and said second cache memories independent of whether said corresponding disk data is included in both said first and said second cache memories,*** as set forth in Claim 1.

For reasons similar to those set forth regarding Claim 1, Applicant's amended Claim 18 is also neither disclosed nor suggested by the references, taken separately or in combination in

that the references neither disclose nor suggest ***a system for managing data in a cache comprising: a first cache memory containing data; a second cache memory containing data wherein at least some of the data contained in the first cache memory is the same as at least some of the data contained in the second cache memory, wherein data contained in said first and said second cache memories includes control data and corresponding disk data, said control data being replicated in said first and said second cache memories independent of whether said corresponding disk data is included in both said first and said second cache memories; and cache selection hardware for selecting, in response to a request for requested data that is stored in both the first cache memory and the second cache memory, which one of the first and second cache memories to use to obtain the requested data in accordance with an access balancing technique,*** as set forth in amended Claim 18.

For reasons similar to those set forth regarding Claim 1, Applicant's amended Claim 31 is also neither disclosed nor suggested by the references, taken separately or in combination in that the references neither disclose nor suggest ***a computer program product stored on a computer readable medium for managing data in a cache, comprising: machine executable code for providing a first cache memory containing data; machine executable code for providing a second cache memory containing data, wherein at least some of the data contained in the first cache memory is the same as at least some of the data contained in the second cache memory, wherein data contained in said first and said second cache memories includes control data and corresponding disk data, said control data being replicated in said first and said second cache memories independent of whether said corresponding disk data is included in both said first and said second cache memories; and machine executable code for, in response to a request for data that is stored in both the first cache memory and the second***

cache memory, selecting which one of the first and second cache memories to use to obtain the requested data in accordance with an access balancing technique, as set forth in amended Claim 31.

In view of the foregoing, Applicant respectfully requests that the rejection be reconsidered and withdrawn.

The rejection of Claims 3 and 33 under 35 U.S.C. § 103(a) as being unpatentable over Dewey in view of Kurokawa and further in view of Mason et al. (PCT/US98/19725, hereinafter referred to as "Mason") is hereby traversed and reconsideration thereof is respectfully requested. Applicant respectfully submits that Claims 3 and 33, as amended herein, are patentable over the cited references.

Claim 3 depends from Claim 1, and Claim 33 depends from Claim 31. For reasons set forth above, Claims 1 and 31 are neither disclosed nor suggested by Dewey and Kurokawa. For reasons set forth below, Applicant respectfully submits that combining Dewey and Kurokawa with Mason also neither discloses nor suggests Claims 1 and 31, and claims that depend therefrom.

Mason relates to mass storage systems in which stored logical volumes are duplicated in mirror form. (See page 1, lines 4-7). Mason describes dynamically adjusting the mirror policy for a disk drive system by periodically collecting statistics for the reading and writing of data to

mirrored logical volumes and determining from the collected statistics whether the mirror service policy should continue or change. (See Abstract).

Applicant's Claim 1, as amended herein, is neither disclosed nor suggested by the references, taken separately or in combination, in that the references neither disclose nor suggest ***a method of managing data in a cache, comprising: providing a first cache memory containing data; providing a second cache memory containing data, wherein at least some of the data contained in the first cache memory is the same as at least some of the data contained in the second cache memory, wherein data contained in said first and said second cache memories includes control data and corresponding disk data, said control data being replicated in said first and said second cache memories independent of whether said corresponding disk data is included in both said first and said second cache memories; and in response to a request for data that is stored in both the first cache memory and the second cache memory, selecting which one of the first and second cache memories to use to obtain the requested data in accordance with an access balancing technique,*** as set forth in Claim 1. For reasons set forth above, Dewey and Kurokawa do not disclose or suggest at least the feature of ***wherein data contained in said first and said second cache memories includes control data and corresponding disk data, said control data being replicated in said first and said second cache memories independent of whether said corresponding disk data is included in both said first and said second cache memories,*** as set forth in Claim 1. Mason also appears silent with regard to the feature of ***wherein data contained in said first and said second cache memories includes control data and corresponding disk data, said control data being replicated in said first and said second cache memories independent of whether said corresponding disk data is***

included in both said first and said second cache memories, as set forth in Claim 1. Thus, Mason does not overcome the deficiencies of Dewey and Kurokawa with respect to Applicant's amended Claim 1. Accordingly, the references neither teach, disclose or suggest at least the feature of ***wherein data contained in said first and said second cache memories includes control data and corresponding disk data, said control data being replicated in said first and said second cache memories independent of whether said corresponding disk data is included in both said first and said second cache memories,*** as set forth in Claim 1.

For reasons similar to those set forth regarding Claim 1, Applicant's Claim 31 is also neither disclosed nor suggested by the references, taken separately or in combination in that the references neither disclose nor suggest ***a computer program product stored on a computer readable medium for managing data in a cache, comprising: machine executable code for providing a first cache memory containing data; machine executable code for providing a second cache memory containing data, wherein at least some of the data contained in the first cache memory is the same as at least some of the data contained in the second cache memory, wherein data contained in said first and said second cache memories includes control data and corresponding disk data, said control data being replicated in said first and said second cache memories independent of whether said corresponding disk data is included in both said first and said second cache memories; and machine executable code for, in response to a request for data that is stored in both the first cache memory and the second cache memory, selecting which one of the first and second cache memories to use to obtain the requested data in accordance with an access balancing technique,*** as set forth in amended Claim 31.

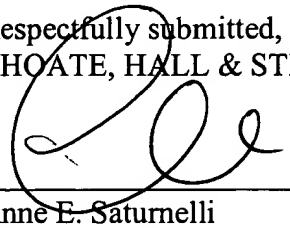
In view of the foregoing, Applicant respectfully requests that the rejection be reconsidered and withdrawn.

In response to the rejection of Claims 1-2, 4-7, 12-32 and 34-37 under the judicially created doctrine of obviousness-type double patenting as being unpatentable over Claims 1-35 of U.S. Patent No. 6,591,335 (the '335 patent) or Claims 1-19 of U.S. Patent No. 6,604,171 (the '171 patent), each taken separately, in view of Kurokawa, Applicant submits herewith a terminal disclaimer. Accordingly, in view of the foregoing, Applicant respectfully requests that the rejection be reconsidered and withdrawn.

In response to the rejection of Claims 3 and 33 under the judicially created doctrine of obviousness-type double patenting as being unpatentable over Claims 1-35 of U.S. Patent No. 6,591,335 (the '335 patent) or Claims 1-19 of U.S. Patent No. 6,604,171 (the '171 patent), each taken separately, in view of Kurokawa, and further in view of Mason, Applicant submits herewith a terminal disclaimer. In view of the foregoing, Applicant respectfully requests that the rejection be reconsidered and withdrawn.

Based on the above, Applicant respectfully requests that the Examiner reconsider and withdraw all outstanding rejections and objections. Favorable consideration and allowance are earnestly solicited. Should there be any questions after reviewing this paper, the Examiner is invited to contact the undersigned at 617-248-4042.

Respectfully submitted,
CHOATE, HALL & STEWART



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